Electrical Bus Prot ction Method & Apparatus

RELATED APPLICATION

This application claims the benefit of priority pursuant to 35 USC 119 of provisional patent application entitled, "Electrical Bus Protection Method & Apparatus", having Serial No. 60/392,651 filed 27 June 2002, and of provisional patent application of same title, having Serial No. 60/411,090 filed 16 September 2002, the disclosures of these applications are hereby incorporated in their entirety by reference herein.

FIELD OF THE INVENTION

The present invention generally relates to power line systems, and more particularly to an apparatus and method for protecting an electrical power line bus or other electrical conductors having a plurality of power or electrical energy transmission lines that transmit currents. More specifically, the invention relates to a signal processing scheme intended to prevent (block) false tripping by a bus protection protective relay due to miss-information derived from saturated current transformers connected to a bus protection relay.

BACKGROUND OF THE INVENTION

Electrical power transmission line systems are of course well known. An exemplary system is shown and described in US Patent 6,307,703, entitled, "Parallel-Feeder Directional Overcurrent Protection, issued to Hindle, et al, herein incorporated by reference thereto. Many such protection systems are

known in the art, as exemplified by US Patent, *6,369,996, entitled,* "Fault Protection Scheme," issued to Bo, herein incorporated by reference thereto.

Before proceeding, power lines or feeder lines, as used herein, refers to any electrical current transmitting line coupled to the bus for transmitting current either from equipment generators or delivered to equipment loads, and the like.

Bus protection relays are also well known. One example of a bus protection relay is shown and described in the attached product brochure known as "B-PRO," Model 8700/BUS, manufactured by NxtPhase Technologies, SRL (formerly APT Power Technologies), the attached brochure being incorporated herein by reference thereto.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a method and apparatus for protecting an electrical power line bus having a plurality of feeder lines coupled thereto.

Another object of the present invention is to provide a method and apparatus for protecting an electrical power line bus having a plurality of feeder lines, including those connected or coupled to loads and equipment, where each bus is associated with one of a plurality of phase identified transmission lines – commonly a 3-Phase Power Line System.

In accordance with the present invention, monitoring signals representative a respective one of the electrical characteristic of the current associated with each one of the power lines, e.g., feeder or equipment or generator lines, coupled to an

electrical power line bus are signal processed in such a manner so as to derive a trip signal indicative of a fault condition so as to protect the bus from damage.

In accordance with the present invention, a protection relay if provided for a power line system for protecting a bus. The bus is provided for transmitting current to and from one or more power lines for receiving and generating power, and where associated with each of the power lines is a current transformer for providing a line signal current representative of current flowing through a respective line. The protection relay is operative for generating a trip signal in response to a detected power signal line fault. In the present invention, the protection relay includes a signal processor responsive to signal line currents for generating a trip signal in response to a detected fault on any one of power lines. Further, means is provided responsive to the signal line currents for detecting current transformer saturation; and selectively generating a blocking signal for blocking the usual trip signal in response to detection of current saturation of the current transformer. In the preferred embodiment of the present invention, current saturation detection is provided by way of monitoring a phase value of a selected harmonic of signals derived from the all of the power line currents, associated with a single bus associated with a single phase.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a schematic block diagram of a bus protection system for one phase of a multi-phase power system and where a bus in coupled to a plurality of power lines.

Figure 2 is a block diagram of the method in accordance with the present invention.

Figure 3 is a graphical depiction of block and hold region of the bus protection in accordance with the present invention to prevent false tripping in the case where current transformer saturation occurs late after fault initiation.

DETAILED DESCRIPTION OF THE INVENTION

In accordance with the present invention, the bus protection system includes a saturation detector that will detect all CT saturation conditions for external faults and block the differential protection from operating, when this condition occurs. Further the signal processing in accordance with the present invention is intended to be immune to partial or fully offset waveforms, harmonics, fault arcing resistance, capacitive or inductive loads, severity of saturation, speed at which saturation occurs, and CT saturation occurring during only a portion of a detected fault. The saturation detection in accordance with the present invention is intended to not interfere with internal faults (with or without saturation), not affect the operating speed of the bus-protection differential current detection function, and not require any special settings. Further, the bus protection system in accordance with the present invention is intended to be simple to use and may be enabled or disabled. Once enabled, a timer may be set to control how long an external current transformer saturation condition is permitted to block the differential protection - normally this timer may be set to be slightly longer than the maximum clearing time for an external fault.

The signal processing scheme in accordance with the present invention is intended to prevent (block) false tripping by a bus protection protective relay due to miss-information derived from saturated current transformers connected to the relay. In a conventional protection relay, saturated current transformer information may appear to be overall current imbalance – when in fact there is none – and cause a highly undesirable false trip.

Figure 1 illustrates a protective relay 5 connected to a power system bus1 in a conventional manner. It should be recognized that Figure 1 illustrates a three phase system. Current transformers (CT) 3 provide current signals associated with a respective one feeder line – only one is numerically identified in the drawing. Protective relay 5 includes signal processing for arriving at a trip decision signal in response to received current signals from the CT is a conventional manner.

Before proceeding, it should be recognized that protection relay 5 includes a variety of electrical components commonly including analog-to-digital transformations, a microprocessor for providing a variety of protective elements for monitoring power line currents derived from the current transformers employing a variety of logically combined algorithms as well known, Such systems are commonly commercially available by Schweitzer Engineering Laboratories, as well as the aforesaid "B-PRO," Model 8700/BUS, manufactured by NxtPhase Technologies, SRL (formerly APT Power Technologies), the associated brochure being incorporated herein by reference thereto.

Figure 2 illustrates a signal processing scheme by way of the block diagram shown therein, and may be incorporated by hardware, firmware,

software, and the like, in order to provide the trip decision signal 6. The signal processing system in accordance with the present invention utilizes several derived characteristics of the feeder currents.

In a conventional manner, both the phasor sum of the power line currents associated with the power lines coupled to the bus, and the magnitude sum of these currents are first determined – equations 1. In turn, the derivatives of the phasor sum and magnitude sum signal are determined – equations 2. A harmonic of the derivative expressions, more specifically the second harmonic, is derived – equations 3. In turn the phase between the second harmonics of the derivatives of the phasor sum signal and magnitude sum signal is determined and compared to a selected threshold, e.g., "5" – equations 4. This comparison is then used to generate a block tripping signal, 6 as illustrated in Figure 1.

Figure 3 illustrates another aspect of the present invention, and is referred to by way of the last two blocks in block diagram illustrated in Figure 2. To allow for the case where current transformer saturation occurs several cycles after fault initiation, a subsidiary BLOCK AND HOLD SIGNAL is generated. The BLOCK AND HOLD SIGNAL is indicative of the data pair consisting of the phasor sum signal Io and magnitude sum signal Ir falling within the shaded area of Fig. 3.

The BLOCK AND HOLD signal is a "trip blocking signal" that is held for several cycles beyond the time at which late saturation is detected, since otherwise, the perceived fault trajectory may cause a false trip.

The following mathematical descriptions depict the equations 1-4 referred to in the above exposition.

Equations 1 - The Calculation of IO (phasor sum) and IR (magnitude sum)

The equations for the calculation of IO and IR (for phase A, B, and C respectively)

$$IOa = \sum_{i=1}^{M} IA_i \qquad IOb = \sum_{i=1}^{M} IB_i \qquad IOc = \sum_{i=1}^{M} IC_i$$

$$IRa = \frac{1}{2}\sum_{i=1}^{M} IA_i \qquad IRb = \frac{1}{2}\sum_{i=1}^{M} IB_i \qquad IRa = \frac{1}{2}\sum_{i=1}^{M} IC_i$$

where **M** is the number of power line inputs connected to the bus; **IA, IB** and **IC** are the fundamental power line current phasors (i.e. vector: a complex number).

Equations 2 - The Calculation of Derivative of IO and IR

$$dIOa\_dIt_n = dIOa\_dt_{n-1} \cdot \left(1 - \frac{\Delta t}{TW}\right) + \frac{(IOa_n - IOa_{n-1})}{TW} \cdot K$$

$$dIRa\_dIt_n = dIRa\_dt_{n-1} \cdot \left(1 - \frac{\Delta t}{TW}\right) + \frac{(IRa_n - IRa_{n-1})}{TW} \cdot K$$

The above equations are only showed for phase A current signals associated with connected or coupled loads and equipment currents. Similar equations may be expressed for phase B and phase C load and equipment currents as should be understood by those skilled in the art.

Where **TW** is a smoothing time constant, **K** is a scaling factor, and subscript "**n**" is an indication of the present value, and "**n-1**" is the value of one time step before. Δ**t** is the time step.

Equations 3 - The Calculation of the Second Harmonics Phasor of the Derivative of IO and IR

$$HDft\_dIOa\_dt_n = \frac{2}{N} \cdot \sum_{i=0}^{N-1} dIOa\_dt_{n-i} \cdot e^{-j \cdot \frac{2 \cdot \pi \cdot i}{N}}$$

$$HDft\_dIRa\_dt_n = \frac{2}{N} \cdot \sum_{i=0}^{N-1} dIRa\_dt_{n-i} \cdot e^{-j \cdot \frac{2 \cdot \pi \cdot i}{N}}$$

where N is the half of the number of samples of the fundamental frequency, e.g., a 50Hz or 60Hz cycle. Phase B and Phase C are similar.

Equations 4 - The calculation of the Phase Difference between HDft_dIO_dt$_n$ and HDft_dIR_dt$_n$

The phase difference is calculated through the product of **HDft_dIO_dt$_n$** and the conjugate of

HDft_dIR_dt$_n$, i.e.

$$\text{Dot ProdOfdIOa\_dIRa}_n = \text{HDft\_dIOa\_dt}_n \bullet \text{HDft\_dIRa\_dt}_n^* \text{ \{the conjugate\}}$$

$$\tan(Pha_n) = \frac{\mathrm{Im}(\mathrm{ProdOfdIOa\_dIRa}_n)}{\mathrm{Re}(\mathrm{ProdOfdIOa\_dIRa}_n)}$$

Where the superscript * represents the conjugate of a complex number, **Im** is to extract the imaginary part of the complex number, and **Re** is to extract the real part of the complex number.

When **$\tan(\mathrm{Pha}_n) > T$**, issue a blocking signal to the differential protection function; otherwise do not block the differential protection. "**T**" is a preset value.

Phase B and Phase C are similar.

The bus protection system in accordance with the present invention includes a significant improvement to the traditional two slope differential characteristic that provides immunity to CT mismatch and minimal CT saturation sensitivity for external faults.

It should be recognized that the aforesaid calculations and signal processing may be accomplished digitally by way of simple programming within the exiting systems well within the level of those skilled in the art within existing common well known protection relays similar to those as already described without additional hardware, and the like.